Amendments to the Specification:

Please replace the fifth paragraph, page 5, starting line 16, with the following:

Referring to Figure 2, the equipment of the present invention comprises analyser software 100 and test software 102, which are run on a computer 110 that is connected via an adapter [[112]] 105 to a board 120 that is to be tested. The test software 102 is stored in a high level language as described below. Loaded into the computer 100 are boundary-scan description language (BSDL) files 111, a netlist 112 and a set of test scripts 114. Beside the netlist 112 is shown a connections list 113.

At page 7, line 9, replace "pad the connector 112" with –via the adapter 105—

At page 8, lines 11 and 14, replace "connector 112" with –adapter 105—

Please replace the second paragraph, page 7, starting line 7, with the following:

The ~~connector 112~~ adapter 105 is a USB-to-JTAG converter that need not be described in detail.

Please replace the fifth paragraph, page 7, starting line 27, with the following:

An example of a typical data structure is given below, and by way of brief explanation a typical operation of the software will be the performance of a test, which may be a connection test 201 or an IC-specific script 114 which will set a pin to a given number. This instruction is compiled by the compiler 206 into a set of instructions that write data using the JTAG chain to internal variables and call the JTAG engine. The JTAG engine works through the netlist to find the best place from which to drive the desired pin and drives that pin by "writing" a JTAG chain that will set the necessary pins to perform the test. The software 102 performs a call which will

read back a result from the selected pins and determine whether the test has passed or failed. The above steps are repeated to complete an entire test sequence. To further illustrate the preferred embodiment, an example of a circuit to be tested is illustrated in Figure 4. In this example, there are two JTAG-capable ICs 401 and 402, which are connected to a non JTAG IC 403, which is further connected to another non-JTAG IC 404. Connected to the first of these ICs is a test data input (TDI) line 410, a test clock (TCK) line 412 and a test mode select (TMS) line 414. The TMS and TCK lines are also connected to IC 402. The TDI line 410 is connected to a TDI input of IC port 401. Lines 410 to 414 are connected to the processor 110 ~~pad the connector 112~~ via the adapter 105. A further line 416 connects a test data output (TDO) of IC 401 to a TDI of IC 402. A TDO for IC 402 emerges at the bottom of the Figure as line 418. This may be connected to a further JTAG-capable device to continue the chain, or it may be connected to the ~~connector 112~~ adapter 105 for returning data to the processor 110.